

INFORMATION DISCLOSURE CITATION IN AN APPLICATION							
				ATTY. DOCKET NO. 49657-935	SERIAL NO.		
(PTO-1449)				APPLICANT Niichi ITOH	FILING DATE January 09, 2001		
				GROUP Z1Z4	U.S. PTO 09/756269		
EXAMINER'S INITIALS PATENT NO. DATE NAME CLASS SUBCLASS FILING DATE							
eu	5,867,415	Feb. 2, 1999	MAKINO				
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
eu	63-55627	Mar. 10, 1988	JAPAN (with English abstract)				
eu	9-231056	Sept. 5, 1997	JAPAN (with English abstract)				
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
Mg	"A Compact 54X54-bit Multiplier with Improved Wallace-Tree Structure", N. Itoh et al., 1999 Symposium on VLSI Circuits Digest of Technical Papers, pp. 15-16						
Mg	"A Compact 54X54-bit Multiplier with Improved Wallace-Tree Structure", N. Itoh et al., Technical Report of IEICE, Vol. 99, No. 145, June 24, 1999, pp. 9-16						
EXAMINER	Mgo			DATE CONSIDERED	4/15/04		

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.